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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,053	03/16/2001	Eyal Rosin	968/34	4674

7590 05/10/2004

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EXAMINER

TREAT, WILLIAM M

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 05/10/2004

7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/809,053

Applicant(s)

ROSIN ET AL.

Examiner

William M. Treat

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2 and 5.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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1. Claims 1-14 are presented for examination.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-14 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lavi et al. (WO 99/42922).

6. Lavi taught a data processor (Fig. 1) comprising at least one off-core execution unit (61, 62, 63, 64), a CLIW memory (10) for storing at least one CLIW instruction (p. 10, line 36 through p. 11, line 3), and a core processor (elements 1-5, 7-10, and 15) operative to retrieve said at least one CLIW instruction from said CLIW memory and forward at least a respective portion

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of said at least one CLIW instruction to at least one of said at least one off-core execution units (p. 6, line 30 through p. 7, line 13; page 8, lines 8-10; p. 11, lines 5-18). By designating elements 1-5, 7-10, and 15 of Fig. 1 as the core processor, the examiner has made the execution units off-core (in other words, not part of the core processor). The elements recited by the examiner as being the processor core perform the same functions as applicants' processor core. The elements recited by the examiner as being the execution units perform the same functions as applicants' execution units and meet the same limitation of not being part of the processor core. Applicants may have intended off-core to mean not part of a processor core chip but their claim language does not make that distinction. Furthermore, were applicants to make such a distinction clear and to find support for it in their disclosure, it would not render applicants' claims patentable. The examiner takes Official Notice of the fact that there are many reasons for moving functional elements on or off a chip such as conservation of chip real estate, power conservation, limit heat build-up, greater flexibility in design changes, faster processing speed for on-chip because of shorter communication distances and reduced line capacitances, etc. In other words, it is merely a design choice whether a functional element is on or off-chip.

7. As to claim 2, Lavi taught the core processor (elements 1-5, 7-10, and 15) is operative to execute a plurality of instructions (page 11, lines 11-18) and one instruction executed by the core processor is the Reference Instruction for initiating retrieval and execution of said CLIW instruction (page 11, lines 5-18).

8. As to claim 3, Lavi taught the data processor (Fig. 1) further comprising a data memory (3) and a data address logic system (4) operative to control access to the data memory by the core processor and off-core execution unit. (Note that the only address lines for accessing the data

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memory are the lines "m" from the address decoder.) One of ordinary skill in the art would be motivated to use the data address logic system (4) for access by both core processor and off-core execution unit to preclude producing redundant circuitry and introducing the need for added circuitry to control access by multiple address decoders. Alternatively, there is inherently data address logic circuitry in the data processor to control access to the data memory by both core processor and off-core execution unit and the totality of such circuitry in the Lavi system meets applicants' claim limitation whether that is only element 4 or not.

9. As to claim 4, Lavi taught the core processor is operative to retrieve the CLIW instruction from CLIW memory, and said data address logic is operative to control access to said Data Memory by said core processor and to said Data Memory by said at least one off-core execution unit, substantially simultaneously (page 7, lines 4-13).

10. As to claim 5, Lavi taught a CLIW instruction decoder (9), and said data address logic is operative to control access to said data memory by said core processor and to said Data Memory by said at least one off-core execution unit, substantially simultaneously (page 7, lines 4-13).

11. As to claims 6-14, there are merely the limitations of claims 1-5 couched in method language, and as such, they fail to teach or define over rejected claims 1-5.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

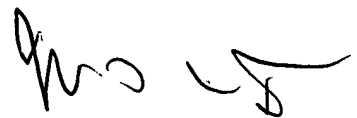
13. Pechanek et al. (Patent No. 6,467,036).

14. Any inquiry concerning this communication should be directed to William M. Treat at telephone number 703 305 9699. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number.

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The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**WILLIAM M. TREAT
PRIMARY EXAMINER**